FIVE LAYER ADHESIVE/INSULATOR/METAL/ INSULATOR/ADHESIVE TAPE FOR SEMICONDUCTOR DIE PACKAGING

RELATED APPLICATION

[0001] This application is a divisional of U.S. Patent Application Serial No. 09/860,304, filed May 18, 2001, now allowed, which is based upon and claims priority to U.S. Provisional Application Serial No. 60/205,726, filed May 19, 2000.

FIELD OF THE INVENTION

[0002] This invention relates to semiconductor die packaging and more specifically relates to a novel five-layer tape which enables the mounting and interconnection of plural semiconductor die relative to one another and to a lead frame support.

BACKGROUND OF THE INVENTION

[0003] Metallization-on-tape is a type of an interconnect that is routinely used in the semiconductor industry in various applications such as tape-automated bonding (TAB). The use of polymer film for this purpose, such as polyimide as an insulative layer, is also known and is used in many semiconductor packaging solutions. Placing an adhesive layer on the film is also used to bond interconnects or insulation layers to the substrate and/or semiconductor die.

[0004] However, all three elements - adhesive layers, insulative layers (such as polyimide film) and metallic fingers/interconnect have not been previously combined in a single tape.

BRIEF DESCRIPTION OF THE INVENTION

[0005] In accordance with the invention, a novel five-layer sandwich of adhesive, insulation, metal, insulation and adhesive layers provides a whole new variety of potential applications such as bonding, interconnection and mutual insulation of different parts of the semiconductor package at the same time. In order to have a contact with a terminal on the semiconductor die or other bonding pad site, windows are formed in the insulative layer. Then thermocompression, for example, can be used to as a means to connect the metallic layer of the tape to the bonding site by conventional means. The novel tape can be produced, using a double-side adhesive insulative tape (for example, a polyimide film coated with adhesive) with windows formed in the film at designated sites where connection is to take place. A metallic layer is deposited/pressed down/glued onto the insulation layer as desired. Finally a single-sided or double-sided adhesive-coated insulated layer (also with pre-cut windows if desired) is pressed on top of the metallic layer and the first insulative layer to produce the finished tape. The tape may be unreeled from a supply reel of any desired length, and then cut off in pieces of size suitable for a given application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a cross-section of the novel 5 layer tape of the invention.

[0007] Figure 2 shows in cross-section, the formation of a window in the tape to permit connection to a semiconductor die electrode gold bump.

[0008] Figure 3 shows the steps which can be used to bury and form terminals for a conductive trace in the novel five layer film.

[0009] Figure 4 shows a prior art die-on-die and a wire-bonded semiconductor package.

[0010] Figure 5A, 5B and 5C show the steps in forming a novel die-on-die package using the novel tape of the invention.

[0011] Figure 6A, 6B and 6C show the steps in forming a side-by-side die arrangement which can be used, for example, for a half-wave bridge circuit configuration.

DETAILED DESCRIPTION OF THE DRAWINGS

[0012] Figure 1 is a sectional view of the novel five layer tape of the invention. Thus, tape 10 consists of a first layer 11 of adhesive; a second layer 12 of an insulation material, for example, Kapton; a third layer 13 of metal, for example, copper or a copper alloy; a fourth layer 14 which is an insulator layer and may be identical in structure to layer 12 and a fifth layer 15 of adhesive that may be identical to layer 11.

[0013] The layer thicknesses are sufficiently thin to enable flexing of the tape body 10, for example, to be rolled into and form a reel and to allow for easy cutting to size by conventional shearing mechanisms used in TAB and other existing processes. Further, the material 10 may have any desired length and width.

[0014] The central conductive layer 13 may have the full area of the other layers, or can be formed as one or more traces of predetermined length and pattern. In order to connect layer 13 to a semiconductor die terminal or some other bonding pad site, windows are formed in the insulation layers 12 and 14, and adhesive layers 11 and 15 as desired. A thermocompression bonding site may exist at the exposed area of metal layer 13. Thus as shown in Figure 2, a connection is made to a gold terminal bump 20 on silicon die 21. To affect this connection, a window 22 is cut into layers 11 and 12 so that, with compression, the top of bump 20 will engage and electrically contact the exposed bottom surface of metal layer 13. The assembly 10 is pressed down forcefully to cause adhesive layer 11 to engage and adhere to the top surface of die 21, holding the bump 20 and metal layer 13 in good low resistance contact.

[0015] Obviously, plural windows placed in different areas of the body 10 and on opposite surfaces thereof to metal 13 will enable the interconnection of a plurality of terminals of the die 21 and of other die (not shown) and of the die support structure.

[0016] Figure 3 shows, in steps A, B, C and D one method for making the body or tape 10. Thus Figure 3A shows the starting body 30 which is a thin insulation sheet, for example, any desired polyimide having adhesive layers coated on both of its surfaces. Windows 31, shown in Figure 3B are then cut, for example, by a stamping die tool 32 in sheet 30. Any desired number of windows can be formed, depending on the end application or package.

[0017] A metal interconnect layer or trace 33, shown in Figure 3C is then formed atop the adhesive surface of sheet 30, overlapping window 31. Layer 33 may have any desired configuration, shown as a convoluted trace in Figures 3C and 3D and may be a foil pressed onto the adhesive surface of layer 30; or may be otherwise formed or deposited.

[0018] Next, and as shown in Figure 3D, a sheet 40, which may have adhesive on its lower surface and preferably on both of its surfaces, is pressed on top of and adheres to sheet 30 and metal interconnect 33. Sheet 40 may also have windows, such as window 41 which, in the final assembly, will overlay metal trace 33 to make possible a connection of one terminal at window 31 to a second terminal at window 41.

[0019] Figure 4 shows a prior art die-on-die bonded package that can be improved by the tape of the present invention.

[0020] Die-on-die bonding is a known way to arrange several die in a co-pack type device. This bonding technique has several advantages over the conventional side-by-side bonding including higher device density, lower isolation requirements and the potential for a smaller resulting device size. A typical co-pack, shown in Figure 4, includes two die - one power transistor die 50 (such as

MOSFET), and an IC controller die 51. Die 50 is mounted with its drain contact metal on the conductive paddle 52 of a lead frame. The IC die 51 is then mounted on the top surface of die 50. Wire bonds from the output terminals 53 and 54 of the IC die 51 are connected to the exposed gate and source terminals 55 and 56 of power MOSFET 50 (the drain of which is connected to flag 52).

[0021] The die-on-die solution of Figure 4 can be used only if IC controller die 51 is much smaller than the MOSFET die 50; then IC 51 is bonded on top of the MOSFET 50 and selected terminals of the MOSFET 50 can be wired to selected terminals of the IC controller by conventional wire-bonding methods. If the IC controller die 51 is as large as or larger than die MOSFET 50, the described solution is not feasible, since the MOSFET contacts 55, 56 would be underneath the IC 51 and wire bonding can not take place.

[0022] With the novel tape 10 of the invention, the device of Figure 4 can be housed in a die-on-die configuration even though IC die 51 is larger in area than MOSFET die 50. Thus, it becomes possible, with the invention, to, in effect, move the MOSFET bonding pads outside the outline of die 50 and on to the flag 52. This structure is best shown in Figures 5A, 5B and 5C in which parts similar to these of the preceding Figures have the same numerals.

[0023] Thus, in Figure 5A a MOSFET die 60, of smaller area than that of IC die 51 of Figure 4, has its bottom drain contact soldered or otherwise connected to flag or paddle 52 of the device lead frame. An elongated tape 70 of the structure previously described above, has two elongated buried metal strips 71 and 72 which extend from respective windows 73 and 74 (on the bottom of tape 70 to windows 75 and 76 on the top of the tape as shown in Figure 5B. An enlarged IC die or chip 80, shown in Figure 5C is then adhered to the top of die 60 in Figure 5B, obscuring the die 60 and its gate and source terminals. These terminals however are accessible through tape windows 75 and 76, and conduction strips 71 and 72. Thus, wire bonds

78 and 79 can make connection from the IC output terminals 53 and 54 to the masked MOSFET source and gate terminals that are located under the IC die 80.

[0024] Obviously, the concept of moving terminals laterally from die to mounting structure has many applications other than that of Figure 5C.

[0025] Figures 6A, 6B and 6C show the steps for using the novel 5 layer tape of the invention for supporting two die from a common conductive substrate and connecting their terminals to define a bridge circuit. In this circuit, the drain of one device is connected to the conductive substrate while the drain of the other is insulated from the substrate. Such devices have been copacked, but structures such as split lead frames have been needed. The present invention makes it possible to use a common lead frame paddle, using a single strip of tape.

[0026] Thus, Figure 6A shows flag 52 which receives the bottom drain contact of a first MOSFET 100 having source and drain bump contact terminals 101 and 102 respectively. A single sheet 103 of the novel five layer material is prepared with embedded conductor strips 104 and 105, windows 106 and 107 in its bottom layers and windows 108 and 109 in the top layers at the other end of the strip. The strip is pressed into adhesive contact with the top of die 100 and the top of flag 52 and ball contacts (such as ball 110 in the Figure 6B inset) are pressed into contact with the conductive strips 104 and 105.

[0027] As next shown in Figure 6C, a second MOSFET die 120 is placed atop the sheet 52 and is pressed down to contact the tops of one or both conduction 104, 105, through windows 108 and 109 to connect the source of die 100 to the drain of die 120. Separate connectors or bonds can be made to the gates of die 101 and 120.

[0028] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.